Docket No. 0756-1881

#38
5/6/03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of)	Art Unit: 2815
Hongyong ZHANG et al.)	Examiner: E. Lee
Serial No. 09/190,618)	
Filed: November 12, 1998)	
For: SEMICONDUCTOR DEVICE AND)	
METHOD OF FABRICATING)	
THE SAME)	

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with The United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on 5-23-03

Adele M Stamper

RESPONSE

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The Official Action mailed January 23, 2003 has been received and its contents carefully noted. Filed concurrently herewith is a *Request for One Month Extension of Time*, which extends the shortened statutory period for response to May 23, 2003. Accordingly, the Applicants respectfully submit that this response is being timely filed.

The Applicants note with appreciation the consideration of the Information Disclosure Statements filed on November 12, 1998, December 17, 1998, October 10, 2000, January 3, 2001, March 12, 2001, August 24, 2001, September 24, 2001, May 13, 2002, and November 6, 2002.

Claims 1-25, 34-39, 41 and 42 are now pending in the present application, of which claims 1, 6, 11, 16, 19, 37 and 42 are independent. For the reasons set forth in detail below, all claims are believed to be in condition for allowance.

A broad concept of the present invention is a semiconductor device that includes an active matrix circuit having at least one first thin film transistor, and a driving circuit having at least one second thin film transistor, each of the first and second thin film transistors comprising a semiconductor film including a channel forming region, a pair of first regions containing an impurity for giving one conductivity type thereto with the channel forming region therebetween, and a pair of second regions in which a

concentration of the impurity is smaller than that in the first regions, wherein the second regions are interposed between the channel forming region and the pair of first regions, and wherein a distance between the channel forming region and the pair of first regions of the first thin film transistor is greater than that of the second thin film transistor.

Paragraph 2 of the Official Action rejects claims 1-4, 6-9, 12-14, 16-22, 24, 25, 34-38, 41 and 42 as obvious based on the combination of U.S. Patent No. 5,323,042 to Matsumoto and U.S. Patent No. 5,412,493 to Kunii et al. The Applicants respectfully traverse the rejection because the Official Action has not made a *prima facie* case of obviousness.

As stated in MPEP §§ 2143-2143.01, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. "The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." In re Kotzab, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

The prior art, either alone or in combination, does not teach or suggest all the features of the independent claims. Matsumoto and Kunii do not teach or suggest a distance between the channel forming region and the pair of first regions of said first thin film transistor is greater than that of said second thin film transistor.

The Examiner concedes that "Matsumoto does not disclose the distance between the channel forming region and the pair of first regions of said first thin film

transistor being greater than that of said second thin film transistor" (p. 2, Paper No. 36). The Examiner asserts that "it was well known in the art at the time of the invention that active matrix pixel TFTs were susceptible to charge leakage" (Id., citing col. 13, lines 46-61 of Kunii). The Examiner further asserts that "it would have been obvious to one of ordinary skill in the art at the time of invention to increase the length of the low level impurity region (and therefore increase the distance between the channel forming region and the pair of first regions) in the first thin film transistor in order to suppress charge leakage prevalent in the matrix pixel TFT" (Id.).

Regarding the Examiner's assertion, the Applicants understand that, according to Kunii, charge leakage of the matrix pixel TFT is suppressed by increasing the length of the low level impurity region. However, it appears that Matsumoto and Kunii do not teach or suggest any relation between a length of a low level impurity region in a first thin film transistor in an active matrix circuit and a length of a low level impurity region in a second thin film transistor in a driver circuit. That is, even if Kunii teaches that the length of the low level impurity region should be increased, Kunii fails to disclose or suggest that such length should be increased to some length greater than that of a second TFT in a driver circuit.

Also, as noted at pp. 10-11 of the *Amendment* filed November 6, 2002, in Kunii, a length of first and second lightly doped regions 61 and 62 is set to 1μm, the length of a third lightly doped region 63 is set to 0.5μm and the length of a fourth lightly doped region 64 is set to 1.5μm. However, Matsumoto does not disclose the length of the low impurity regions. Thus, it is impossible to draw any comparison between the LDD regions of Matsumoto and Kunii.

Therefore, the Applicants respectfully submit that Matsumoto and Kunii, taken alone or in combination, fail to disclose or suggest that a distance between the channel forming region and the pair of first regions of said first thin film transistor is greater than that of said second thin film transistor. Since Matsumoto and Kunii do not teach or suggest all the claim limitations, a *prima facie* case of obviousness cannot be maintained. Accordingly, reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) is in order and respectfully requested.

Paragraph 3 of the Official Action rejects claims 5, 10, 15 and 23 as obvious based on the combination of Matsumoto, Kunii and U.S. Patent No. 5,028,551 to Dohjo et al. Dohjo does not cure the deficiencies in Matsumoto and Kunii. The Official Action relies on Dohjo to teach multiple layers that consist of tantalum (p. 4, Paper No. 36). Matsumoto, Kunii and Dohjo, either alone or in combination, do not teach or suggest a distance between the channel forming region and the pair of first regions of said first thin film transistor is greater than that of said second thin film transistor. Since Matsumoto, Kunii and Dohjo do not teach or suggest all the claim limitations, a *prima facie* case of obviousness cannot be maintained. Accordingly, reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) is in order and respectfully requested.

Paragraph 4 of the Official Action rejects claim 11 as obvious based on the combination of Matsumoto, Kunii and U.S. Patent No. 5,430,320 to Lee. Lee does not cure the deficiencies in Matsumoto and Kunii. The Official Action relies on Lee to teach a TFT comprising silicon oxide films over a gate electrode (Id.). Matsumoto, Kunii and Lee, either alone or in combination, do not teach or suggest a distance between the channel forming region and the pair of first regions of said first thin film transistor is greater than that of said second thin film transistor. Since Matsumoto, Kunii and Lee do not teach or suggest all the claim limitations, a *prima facie* case of obviousness cannot be maintained. Accordingly, reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) is in order and respectfully requested.

Paragraph 5 of the Official Action rejects claim 39 as obvious based on the combination of Matsumoto, Kunii and JP 56-40269 to Iizuka. Iizuka does not cure the deficiencies in Matsumoto and Kunii. The Official Action relies on Iizuka to teach doping a polycrystalline Si layer with O or N ions (pp. 4-5, Id.). Matsumoto, Kunii and Iizuka, either alone or in combination, do not teach or suggest a distance between the channel forming region and the pair of first regions of said first thin film transistor is greater than that of said second thin film transistor. Since Matsumoto, Kunii and Iizuka do not teach or suggest all the claim limitations, a *prima facie* case of obviousness cannot be maintained. Accordingly, reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) is in order and respectfully requested.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact the Applicants' undersigned attorney at the telephone number listed below.

Respectfully submitted,

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